Reduced thermal resistance of the silicon-synthetic diamond composite substrates at elevated temperatures

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The authors report results of experimental investigation of thermal conductivity of synthetic diamond-silicon composite substrates. Although composite substrates are more thermally resistive than silicon at room temperature they *outperform* conventional wafers at elevated temperatures owing to different thermal conductivity dependence on temperature. The crossover point is reached near ~360 K and can be made even lower by tuning the polycrystalline-grain size, film thickness, and interface quality. The reduction of thermal resistance of composite wafers at temperatures, typical for operation of electronic chips, may lead to better thermal management and new *phonon-engineered* methods for the electron mobility enhancement. © *2010 American Institute of Physics*. [doi:10.1063/1.3463455]

Most recently, there was a notable renewal of interest in composite silicon-synthetic diamond (Si-Di) substrates as alternatives to conventional silicon (Si) wafers. It is driven by several factors. First, continuing downscaling of Si complementary metal-oxide semiconductor (CMOS) technology and progress in high-power electronics demand more efficient heat removal to handle the increasing power density and rising temperature (T) of hot spots.[1–3] The high T in the transistor channels translates into degraded mobility, μ, and, as a result, leads to smaller speed and drive current. Second, there was a fast progress in the chemical vapor deposition (CVD) of ultrananocrystalline diamond (UNCD) and microcrystalline diamond (MCD) on Si.[4] It has been demonstrated that UNCD films can be synthesized at temperatures that CMOS devices can withstand.[5] Additional motivations for Si-Di substrates include prospects of hybrid Si–carbon electronics, which would involve different allotropes of carbon, e.g., diamond, diamond-like carbon, carbon nanotubes, and graphene,[6] as well as proposals for the *phonon-engineered* mobility enhancement in nanoscale Si channels with diamond barriers.[7,8]

At the same time, the heat conduction properties of synthetic diamond are not nearly as good as those of crystalline diamond. The thermal conductivity, K, of high-quality single-crystal diamond is ~2200 W/mK.[9] The room-temperature (RT) thermal conductivity of MCD is ~550 W/mK (Ref. 10) while that of UNCD is much smaller than that of Si.[11] The "effective" thermal conductivity, K_{eff}, defined for the whole MCD/Si and UNCD/Si substrates, depends on the polycrystalline-diamond grain size, diamond layer thickness, and interface quality. The surface roughness for MCD is usually much larger than that for UNCD. The rougher interfaces results in higher thermal boundary resistance, which offsets the thermal conductivity increase due to a lager grain size. Considering that RT thermal conductivity of Si is ~145 W/mK it is not clear if incorporation of synthetic diamond can improve the heat removal at the present state of technology for diamond deposition. For this reason, the conventional belief was that one has to wait for improvements in the CVD diamond until the composite Si-Di wafers become practical for CMOS integration from the thermal management point of view.

In this letter, we show that although composite Si-Di substrates have smaller K_{eff} than Si at RT they outperform Si wafers at elevated temperatures. The crossover point is reached in the range ~360–450 K depending on the grain size and thickness of the synthetic diamond. The temperature when the Si-Di substrates become less thermally resistive is near the operating temperature (T~380 K) of electronic chips[12] and substantially lower than the temperature of hot spots in advanced chips.[3]

For this study we used a set of samples with UNCD (Advanced Diamond Technologies) and MCD (sp3 Diamond Technologies) layers grown on conventional 100 mm Si wafers. To study the effect of the grain size and film thickness on thermal conductivity, some of the samples had the same grain size, defined by the growth conditions, but different thicknesses while other samples had the same thickness but different grain sizes. The Si-Di wafers were characterized using the scanning electron microscopy (SEM) and Raman spectroscopy under 488-nm laser excitation. The Raman spectra for MCD and UNCD are qualitatively different. The observed features were in line with reported data.[10] The SEM images confirmed the average grain sizes $d \approx 5-10$ nm for UNCD films [Fig. 1(a)]. The grain sizes for ~1-μm-thick and 7-μm-thick MCD films were $d \approx 0.5-0.8$ μm and $d \approx 1-3$ μm, respectively [Figs. 1(b) and 1(c)].

The thermal conductivity measurements were carried out using the transient planar source (TPS) method.[13,14] We have previously "calibrated"[10,14] our TPS system with the 3-ω method, a standard technique for K measurements of thin films.[15] In TPS method, an electrically insulated flat nickel sensor plays a role of the heater and thermometer simultaneously. It is placed between two pieces of a sample under investigation (see inset to Fig. 2). During the measurement, a current pulse is passed through the sensor, which generates heat. Thermal properties of the material are determined by

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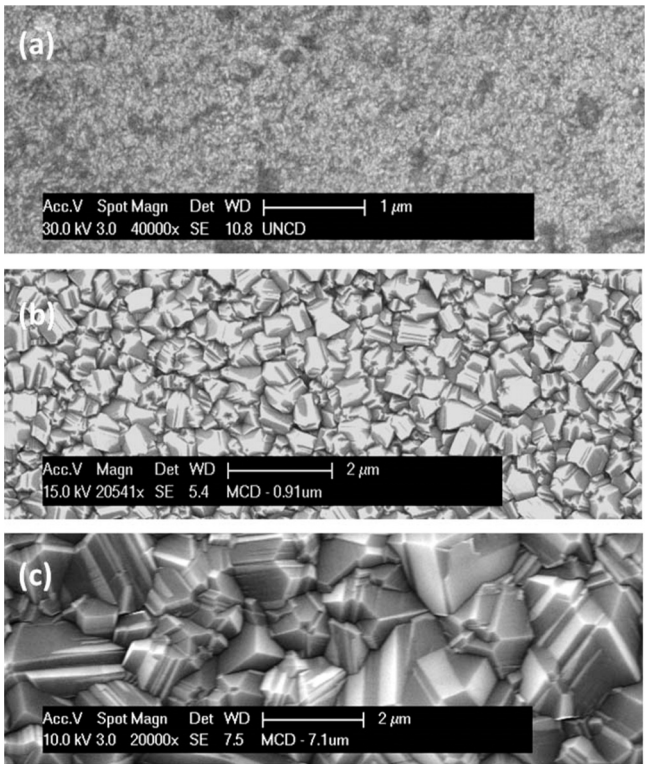

FIG. 1. Top-view SEM images of synthetic diamond films revealing the grain sizes for (a) UNCD film, (b) MCD film with ~1 μm thickness, and (c) MCD film with ~7 μm thickness.

recording temperature rise as a function of time using the equation[13] $\Delta T(\tau)=P(\pi^{3/2}rK)^{-1}D(\tau)$, where $\tau=(t_m\alpha/r^2)^{1/2}$, α is the thermal diffusivity, t_m is the transient measurement time, r is the radius of the sensor, P is the input heating power, and $D(\tau)$ is the modified Bessel function. The time and the input power are chosen so that the heat flow is within the sample boundaries and the T rise of the sensor is not influenced by the outer boundaries of the sample.[13,16,17] In our case, the optimum probing depth was achieved for

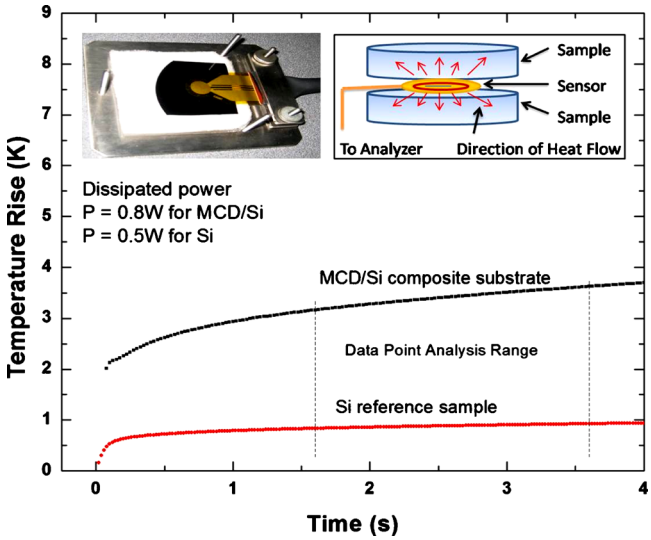

FIG. 2. (Color online) Transient temperature rise for the MCD/Si composite substrate and reference Si wafer used for the thermal conductivity extraction. The insets show the thermal sensor positioned on a sample and schematic of the measurements using TPS technique.

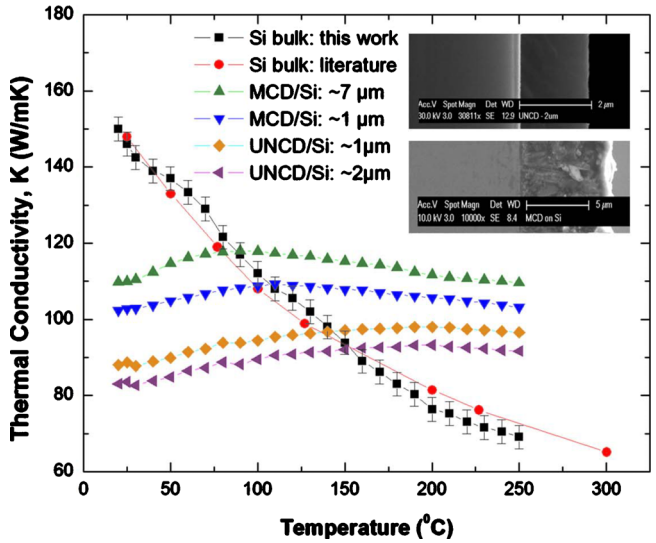

FIG. 3. (Color online) Thermal conductivity as a function of temperature for UNCD/Si and MCD/Si composite substrates, as well as for the reference Si wafer. The insets show the cross-sectional SEM images of UNCD/Si and MCD/Si substrates.

$P=0.8$ W and $P=0.5$ W for the composite MCD/Si and reference Si substrates, respectively (Fig. 2).

Figure 3 presents the measured $K_{\text{eff}}(T)$ for a reference Si wafer, two MCD/Si and two UNCD/Si composite substrates. All examined substrates had distinctively sharp interface between the diamond layer and Si wafer verified by cross-sectional SEM (see inset). A comparison with K values for Si from literature[18] indicates an excellent agreement and attests to the accuracy of our measurements. The Si wafer's K scales as $\sim 1/T$, which is expected for semiconductor crystals near RT. The $K_{\text{eff}}(T)$ dependence for MCD/Si (UNCD/Si) is distinctively different. The thermal conductivity of the composite Si-Di substrates actually grows with temperature from RT to ~100–200 °C, depending on the grain size and thickness of the diamond layer. The unexpected observation is that the crossover point, where K_{eff} of the composite substrates becomes larger than that of conventional Si wafers, is reached at rather low $T\approx 75-150$ °C. The examined MCD/Si substrates start to outperform Si wafers sooner than UNCD/Si substrates. The crossover point shifts to lower T with increasing thickness of MCD layer. This is an important observation, which means that the composite Si-Di wafers can be less thermally resistive at the operating temperature of the state-of-the-art electronic chips and high-power devices.

The physics behind the lower thermal resistivity of Si-Di wafers at elevated temperatures is related to differences in $K(T)$ dependence of crystalline Si and UNCD or MCD. In bulk crystals, K is limited by the crystal anharmonicity via the phonon Umklapp scattering, which results in $1/T$ dependence. In polycrystalline materials K increases with T or depends only weakly on T. The changed T dependence can be explained by various theoretical models, e.g., using a conventional Callaway–Klemens approach, where scattering on grains is the dominant phonon relaxation mechanism,[19,20] or the phonon-hopping model,[21] which predicts higher rates of the phonon grain-to-grain transmissions with increasing T. To analyze our results we determined the thermal conductivity, K_{Di}, of the synthetic diamond layers themselves from the equation $L/K_{\text{eff}}=L_{\text{Si}}/K_{\text{Si}}+L_{\text{Di}}/K_{\text{Di}}$, where $L=L_{\text{Si}}+L_{\text{Di}}$ is the

total thickness of the composite substrate, K_{Si} is the thermal conductivity of the Si wafer, and L_{Si} (L_{Di}) is the thickness of the Si wafer (diamond layer). Here we neglected TBR at the Si/Di interface, which is much smaller than L_{Si}/K_{Si} or L_{Di}/K_{Di} as estimated by applying the above equation to two samples with the same type of diamond layer but different thickness L_{Di}. We then calculated the interfacial grain-to-grain thermal conductance[22] $G=(K_D/d)[1/(K_D/K_{Di}-1)]$, where K_D is the thermal conductivity inside the grain assumed to be equal to the crystalline diamond's bulk value. For our UNCD layers we found $G\sim 50-100$ MW/m^2 K for the grain diameter $d\sim 5-10$ nm at RT. G grows with T and can be approximated as $G(T)(\mathrm{MW/m^2\,K})\approx 81.2+1.65\times 10^{-4}T^3(^\circ\mathrm{C})$ for $d\sim 5$ nm. The $G(T)\sim T^3$ dependence is consistent with the Kapitza thermal resistance behavior.[23] The obtained values fall within the conventionally accepted range $G\sim 20-200$ MW/m^2 K for the interface conductance between dissimilar materials near RT.[24] Our analysis suggests that Si-Di composite substrates even with nonperfect grain interfaces perform better than Si for heat removal at elevated temperatures.

To obtain estimates for the electron mobility enhancement as a result of higher K_{eff} of Si-Di substrates we simulated T profiles in the examined wafers. The heat diffusion equation for given structures was solved numerically by the finite-element method using COMSOL software. The devices were modeled as heat sources with the power density and geometry chosen in such a way so that the resulting temperature rise is close to the typical values in state-of-the-art chips. The Si wafers were then replaced with the Si-Di substrates and modeled with the experimentally determined $K_{eff}(T)$. The difference in the device-channel temperature rise, ΔT_m, between Si wafers and Si-Di substrates was translated into the carrier mobility values using the expression $\mu(T)\sim T^{-n}$, where $n\sim 2.42$ for Si.[25,26] We found that for realistic parameters one can obtain a reduction $\Delta T_m\sim 20-40$ °C, which can result in up to ~20% mobility increase. The μ increase can be made larger via improvement of Si-Di substrates quality, increase in L_{Di} for MCD, and increase in G for UNCD and MCD. The currently used methods for the mobility improvement in Si CMOS use SiGe alloys to strain the device channels.[27] The alloys are characterized by very low K.[28] The mobility, which can be achieved in chips implemented on Si-Di substrates, will not be prone to degradation due to higher thermal resistance. The decrease of the channel temperature due to a lower thermal resistance of the composite substrates at elevated temperatures will also improve chips' reliability and life-time. Another benefit of using diamond with Si is a continuing drive for carbon electronics. Carbon materials are characterized by a very wide range of K, from the highest in graphene[29] to the lowest in disordered carbons,[30] and can provide both thermally conductive and insulating interfaces.

In conclusion, we demonstrated that composite Si-diamond substrates, which are more thermally resistive than Si at RT, *outperform* Si at elevated temperatures characteristic for operation of the high-power and state-of-the-art electronics. The benefits of the composite substrates increase with chips' growing power density and hot-spot temperatures. We elucidated physical processes leading to the improved thermal properties of the composite substrates and outlined the strategy for achieving mobility enhancement via thermal, i.e., phonon flux, engineering.

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